Amendment and Response under 37 C.F.R. 1.116
Applicant: Ashish Gupta
Serial No.: 10/080,440
Filed: February 22, 2002
Docket No.: 10019865-1
Title: SYSTEM AND METHOD FOR MEMORY INTERLEAVING USING CELL MAP WITH ENTRY
GROUPING FOR HIGHER-WAY INTERLEAVING

IN THE CLAIMS

Please cancel claims 29-32.

Please add claims 36-38.

Please amend claims 1 and 34 as follows:

1.(Currently Amended)   A method of accessing a plurality of memories in an
interleaved manner using a contiguous logical address space, the method comprising:

providing at least one map table, the at least one map table including a plurality of
entries, each entry including a plurality of entry items, each entry item identifying one of the
memories;

receiving a first logical address, the first logical address including a plurality of
address bits, the plurality of address bits including a first set of address bits corresponding to
a first set of entries in the at least one map table, wherein each entry in the first set includes
entry items that are different than entry items of other entries in the first set;

identifying a first entry in the first set of entries based on the first set and a second set
of the address bits;

identifying a first entry item in the first entry based on a third set of the address bits;
and

accessing the memory identified by the first entry item.

2.(Original)   The method of claim 1, wherein the first, second, and third sets of address bits
are non-overlapping.

3.(Original)   The method of claim 1, wherein the first, second, and third sets of address bits
are each separated from one another by a plurality of other bits.

4.(Original)   The method of claim 1, wherein the first set of address bits include more
significant bits than the second set of address bits, and wherein the second set of address bits
include more significant bits than the third set of address bits.

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5.(Original)   The method of claim 1, and further comprising:

  storing a plurality of memory offset values in the at least one map table;

  identifying one of the memory offset values based on the first logical address; and

  wherein the memory identified by the first entry item is accessed at a memory
location based at least in part on the identified memory offset value.

6.(Original)   The method of claim 1, wherein the first logical address is a processor address.

7.(Original)   The method of claim 1, wherein the at least one map table is organized into a
plurality of rows and a plurality of columns, and wherein each row corresponds to one of the
plurality of entries and each column within a row corresponds to one of the plurality of entry
items.

8.(Original)   The method of claim 1, and further comprising:

  providing a multi-bit mask value;

  providing a plurality of multi-bit match values;

  extracting the first set of address bits from the first logical address using the multi-bit
mask value; and

  comparing the extracted first set of address bits to the plurality of multi-bit match
values to identify a match.

9.(Original)   The method of claim 1, and further comprising:

  providing at least one multi-bit mask value;

  providing a plurality of multi-bit match values;

  extracting the second set of address bits from the first logical address using the at least
one multi-bit mask value;

  comparing the extracted second set of address bits to the plurality of multi-bit match
values; and

  wherein the first entry in the first set of entries is identified based at least in part on
the comparison of the extracted second set of address bits to the plurality of multi-bit match
values.

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10.(Original) The method of claim 1, and further comprising:

 providing a plurality of multi-bit mask values;

 providing a plurality of multi-bit match values;

 selecting one of the plurality of multi-bit mask values based on a desired interleave entry size;

 extracting the second set of address bits from the first logical address using the selected multi-bit mask value;

 comparing the extracted second set of address bits to the plurality of multi-bit match values; and

 wherein the first entry in the first set of entries is identified based at least in part on the comparison of the extracted second set of address bits to the plurality of multi-bit match values.

11.(Original) The method of claim 1, wherein the memories each include at least one memory segment, the memory segments organized into groups, the memory segments in each group having a uniform size, and wherein each entry in the at least one map table corresponds to one of the groups of memory segments.

12. – 32.(Cancelled)

33.(Previously Presented)   The method of claim 1, wherein the memories are distributed across a plurality of cells, with each cell including at least one processor, a cell controller, and an input/output device.

34.(Currently Amended)   A system for providing interleaved access to a plurality of memories, the system comprising:

 at least one map table including a plurality of entries, each entry including a plurality of entry items, each entry item identifying one of the memories;

 a controller for receiving a first logical address, the first logical address including a plurality of address bits, the plurality of address bits including a first set of address bits

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corresponding to a first set of entries in the at least one map table, wherein at least one of the entries in the first set includes a plurality of entry items that are different than entry items of other entries in the first set; and

wherein the controller is configured to identify a first entry in the first set of entries based on the first set and a second set of the address bits, and identify a first entry item in the first entry based on a third set of the address bits.

35.(Previously Presented)   The system of claim 34, wherein the controller is configured to access the memory identified by the first entry item.

36.(New)   A method of accessing a plurality of memories in an interleaved manner using a contiguous logical address space, the method comprising:

providing at least one map table, the at least one map table including a plurality of entries, each entry including a plurality of entry items, each entry item identifying one of the memories;

receiving a first logical address, the first logical address including a plurality of address bits, the plurality of address bits including a first set of address bits corresponding to a first set of entries in the at least one map table, wherein at least one of the entries in the first set includes a plurality of entry items that are different than entry items of other entries in the first set;

identifying a first entry in the first set of entries based on the first set and a second set of the address bits;

identifying a first entry item in the first entry based on a third set of the address bits; and

accessing the memory identified by the first entry item.

37.(New)   A system for providing interleaved access to a plurality of memories, the system comprising:

at least one map table including a plurality of entries, each entry including a plurality of entry items, each entry item identifying one of the memories;

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a controller for receiving a first logical address, the first logical address including a plurality of address bits, the plurality of address bits including a first set of address bits corresponding to a first set of entries in the at least one map table, wherein each entry in the first set includes entry items that are different than entry items of other entries in the first set; and

wherein the controller is configured to identify a first entry in the first set of entries based on the first set and a second set of the address bits, and identify a first entry item in the first entry based on a third set of the address bits.

38.(New)   The system of claim 37, wherein the controller is configured to access the memory identified by the first entry item.

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